



S/N 09/945,507

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Leonard Forbes et al.	Examiner:	Son Dinh
Serial No.:	09/945,507	Group Art Unit:	2824
Filed:	August 30, 2001	Docket:	1303.014US1
Title:	FLASH MEMORY WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS		

COMMUNICATION CONCERNING RELATED APPLICATION(S)

MS RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicants would like to bring to the Examiner's attention the following related application(s) in the above-identified patent application:

<u>Serial/Patent No.</u>	<u>Filing Date</u>	<u>Attorney Docket</u>	<u>Title</u>
09/945395	August 30, 2001	1303.019US1	DRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS
09/943134	August 30, 2001	1303.020US1	PROGRAMMABLE ARRAY LOGIC OR MEMORY DEVICES WITH ASYMMETRICAL TUNNEL BARRIERS
09/945512	August 30, 2001	1303.027US1	IN SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS
09/945554	August 30, 2001	1303.028US1	SRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS
09/945500	August 30, 2001	1303.029US1	PROGRAMMABLE MEMORY ADDRESS AND DECODE CIRCUITS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS
10/075484	February 12, 2002	1303.043US1	ASYMMETRIC BAND-GAP ENGINEERED NONVOLATILE MEMORY DEVICE
10/081818	February 20, 2002	1303.045US1	ATOMIC LAYER DEPOSITION OF METAL OXIDE AND/OR LOW ASYMMETRICAL TUNNEL BARRIER INTERPOLY INSULATORS

COMMUNICATION CONCERNING RELATED APPLICATIONS

Serial Number: 09/945,507

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Title: FLASH MEMORY WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS

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Dkt: 1303.014US1

10/177096	June 21, 2002	1303.063US1	GRADED COMPOSITION METAL OXIDE TUNNEL BARRIER INTERPOLY INSULATORS
10/783695	February 20, 2004	1303.019US2	DRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS
10/781035	February 18, 2004	1303.063US2	GRADED COMPOSITION METAL OXIDE TUNNEL BARRIER INTERPOLY INSULATORS
10/788810	February 27, 2004	1303.027US2	IN SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS
10/819550	April 7, 2004	1303.019US3	DRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS

Respectfully submitted,

LEONARD FORBES ET AL.

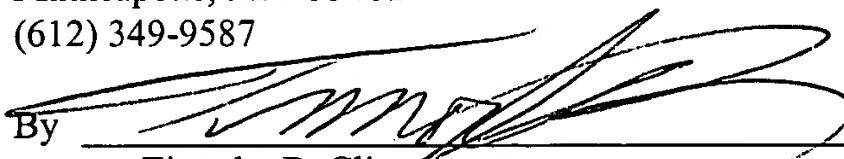
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Date

9 June '04

By



Timothy B. Clise
Reg. No. 40,957

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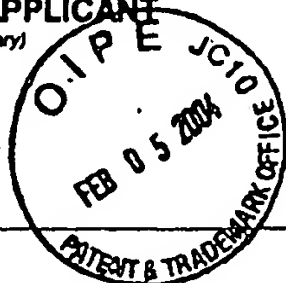
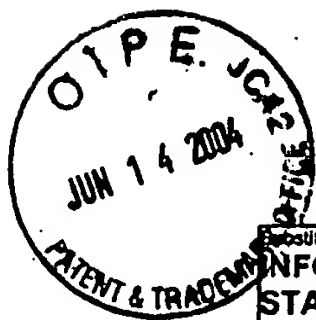
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Tina Kohut

Signature

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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)		Complete if Known	
		Application Number	09/945,507
		Filing Date	August 30, 2001
		First Named Inventor	Forbes, Leonard
		Group Art Unit	2824
		Examiner Name	Dinh, Son
Sheet 1 of 3		Attorney Docket No: 1303.014US1	

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Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date if Appropriate
47	US-2001/0013621	08/16/2001	Nakazato, K	257	314	12/08/2000
	US-2001/0055838	12/27/2001	Walker, A J., et al.	438	129	08/13/2001
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EXAMINER SON DINH

DATE CONSIDERED 3/5/04

Substitute Disclosure Statement Form (PTO-1449)

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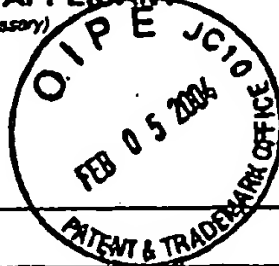
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Substitute for form 1448A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)		Complete if Known <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 40%;">Application Number</td> <td>09/945,507</td> </tr> <tr> <td>Filing Date</td> <td>August 30, 2001</td> </tr> <tr> <td>First Named Inventor</td> <td>Forbes, Leonard</td> </tr> <tr> <td>Group Art Unit</td> <td>2824</td> </tr> <tr> <td>Examiner Name</td> <td>Dinh, Son</td> </tr> </table>		Application Number	09/945,507	Filing Date	August 30, 2001	First Named Inventor	Forbes, Leonard	Group Art Unit	2824	Examiner Name	Dinh, Son
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Filing Date	August 30, 2001												
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Group Art Unit	2824												
Examiner Name	Dinh, Son												
Sheet 2 of 3		Attorney Docket No: 1303.014US1											



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Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T ³

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ³
CD		AARIK, JAAN, et al., "Anomalous effect of temperature on atomic layer deposition of titanium oxide", <u>Journal of Crystal Growth</u> , (2000), pp. 531-537	
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CD		YAMAGUCHI, TAKESHI, "Band Diagram and Carrier Conduction Mechanism in ZrO ₂ /Zr-silicate/Si MIS Structure Fabricated by Pulsed-laser-ablation	

EXAMINER SON DINH DATE CONSIDERED 3/5/14

Substitute Disclosure Statement Form (PTO-1449)

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Sheet 3 of 3	Attorney Docket No: 1303.014US1	

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T*
SD	#	Deposition*, Electron Devices Meeting, 2000. IEDM Technical Digest. International, (2000), 19-22	

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